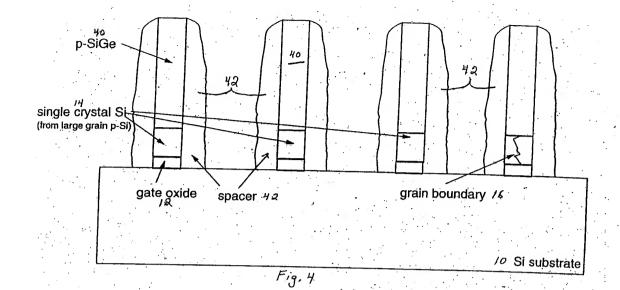


Fig. 3



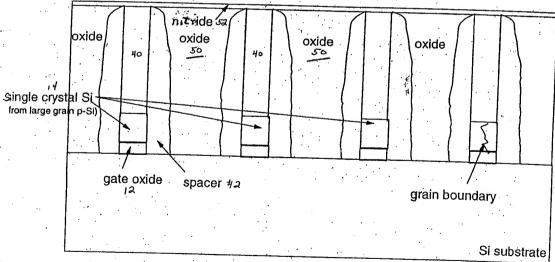
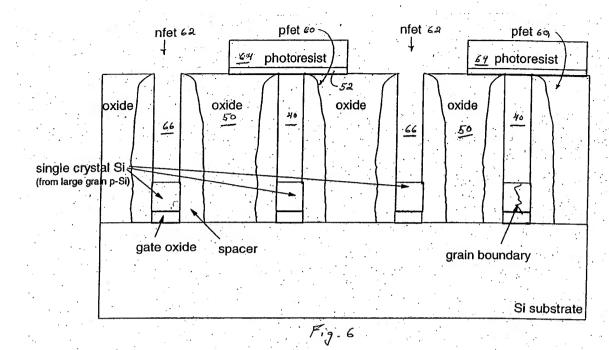
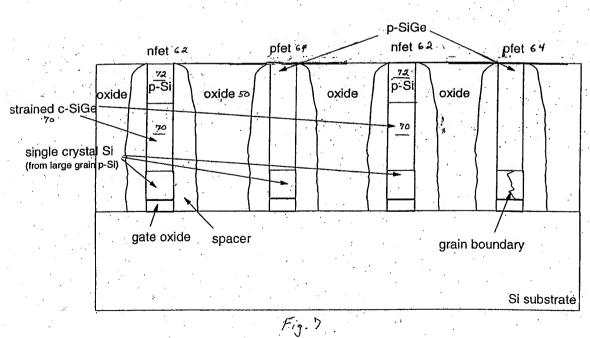
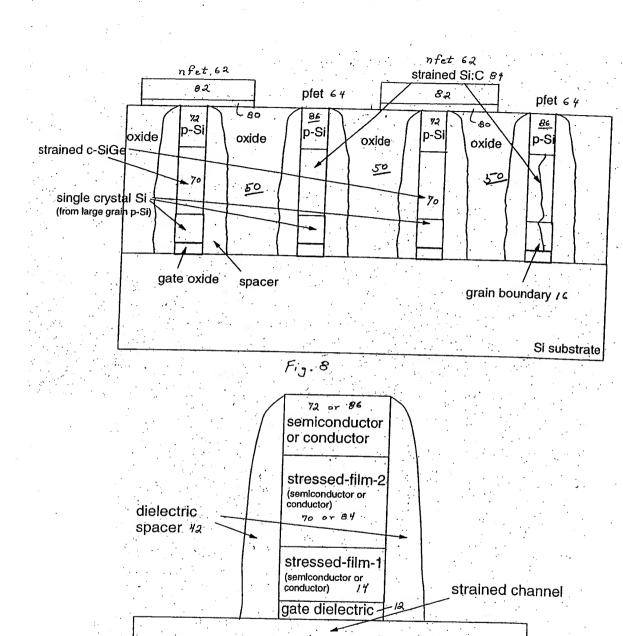


Fig. 5



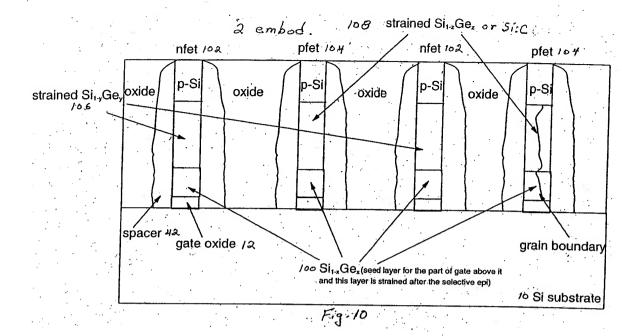




simeconductor oninsulator (sox) 90

simeconductor 10 or

Fig. 9



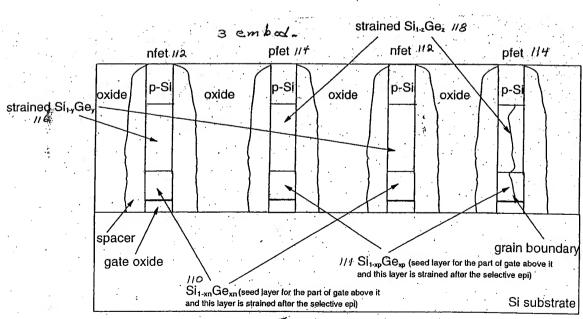


Fig. H.

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## Schematic of layer structure before gate patterning

*	p-Si			*
(this layer could has different stres	Strained SiGe or str	and defferent Ge fra	ctions in nfet and pfet	t regions, separately)
large-grain	n-size p-Si,or p-SiGe, ass levels, different stress types,	is seed for epand defferent Ge in	oi SiGe or Si:C actions in niet and pie	t regions, separately

Si substrate /6

Fig. 12

bonded oxide/Si interface 133

5 em bod.

13a single crystal SOI

gate oxide 131

134 Single crystal

thermal oxide/Si interface 135

13a handle wafer

Fig. 13

a-Si \*/+/+
qate oxide /+/2

///6

c-Si substrate

Fig. 14

